REMARKS

I. Status of Claims

Claims 1-21 are pending.

Claims 1-21 stand rejected.

Claims 1, 8 and 16 are amended herein

II. Objections to the Drawings

The examiner has objected to Figures 1-3 "as they should be labeled PRIOR ART." Revised drawings, which are labeled PRIOR ART, are submitted herewith.

III. Claim Rejections Under 35 U.S.C. § 102(b)

The examiner rejected claims 1-21 as being anticipated by Leung, Pub. No. US 2001/0007538 A1. Leung discloses a memory device wherein "the refreshing of the memory cells does not interfere with any external access of the memory cells." Page 2, paragraph [0011]. While Leung does disclose an embodiment where "daisy-chained connections sequentially pass the refresh request signal to the memory banks" Page 2, paragraph [0013] and Fig. 1 at 1000-1127, the memory refresh system disclosed by Leung does not guarantee that two memory banks cannot be refreshed at the same time.

The refresh requests to sequential memory blocks as disclosed in an embodiment by Leung are one clock cycle apart. See page 4, paragraph [0047]. "The REQO[0] signal is therefore driven high one clock cycle after the REQI[0] signal is activated high. Each

output terminal REQO is connected to an input terminal REQI of a neighboring memory block. The refresh request to the memory blocks is thus generated by a daisy chain formed by the D-registers connecting to the REQI and REQO terminals of the memory blocks 1000-1127." See also page 5, paragraph [0060]. "the input refresh request signal REQI[n] is latched into D-register 321 in response to the rising edge of the Clk signal. D-register 321 provides an output refresh signal REQO[n] to the adjacent memory block in a daisy-chained manner." Note that Leung also discloses an embodiment wherein "the refresh request signal RFREQ is broadcast to all of memory blocks 1000-1127." Page 4 paragraph [0050].

Although Leung discloses refresh requests are daisy-chained from one memory bank to the next, this does not ensure that two or more memory banks will not be refreshed at the same time. That is because "Memory control unit 108 (Figs. 1, 6-9) controls the accessing and refreshing of the memory cells such that refreshing of memory cells does not interfere with any external access of memory cells." Page 9 paragraph [0122]. "When the refresh request signal is activated, a memory bank executes a refresh cycle if there is no access conflict. Otherwise, the refresh cycle is delayed until there is no access conflict." Page 2 paragraph [0013] (emphasis added). The delay can be anywhere from 0 clock cycles up to 256 clock cycles. "A pending refresh in the first memory bank at the beginning of the worst-case access scenario does not get serviced until all 256 cycles later." Page 11 paragraph [0143]. Thus if refresh of bank "a" is delayed one clock cycle and refresh of bank "b," which is daisy-chained to

bank "a," is not delayed, both memory banks will be refreshed simultaneously. Similar effects could cause three or more memory banks to be refreshed simultaneously.

Claim 1. The examiner has cited Leung as disclosing the limitation in claim 1 requiring "sequentially refreshing one or more subsequent memory blocks of the memory system (page 4 paragraph [0047]), wherein all the memory blocks are refreshed within a retention cycle of the memory system (page 1 paragraph [0004])".

Claim 1 as amended herein requires the step of " sequentially refreshing one or more subsequent memory blocks of the memory system such that no two memory blocks are refreshed at the same time." As explained above, Leung neither discloses nor suggests a system wherein no two memory blocks are refreshed at the same time. Because the refresh cycle of any memory block can be delayed in the system disclosed by Leung, (see page 2 paragraph [0013]) it is possible for two or more memory blocks to be refreshed at the same time.

By the claim amendment and the remarks herein, the applicant asserts that the examiner's rejection of Claim 1 has been traversed, and requests that Claim 1 be allowed as presently amended.

Claims 2 - 5 and 7. By the claim amendment to independent Claim 1 and the remarks regarding Claim 1 herein, the applicant asserts that the examiner's rejection of Claim 1 has been traversed, and requests that Claims 2 through 5 and 7, which depend from Claim 1 be allowed.

Claim 6. The examiner has cited Leung as disclosing "refresh commands for the memory blocks [that] do not overlap in timing." (citing page 1 paragraph [0004] and page 2 paragraph [0013]). The overlap in timing prevented by Leung is between refresh cycles and external access to the memory, not between refreshes of memory blocks. "Because an external access and a refresh access can be initiated at the same time, the DRAM array must be able to handle both within the allowable access time so as to prevent the refresh access from interfering with the external access." Page 2, paragraph [0004]. Claim 6 requires that "the refresh commands for the memory blocks do not overlap in timing." While Leung discloses refresh requests that are daisy-chained (page 2 paragraph [13]) Leung does not disclose or suggest that the refresh commands for the memory blocks do not overlap in timing. In fact, in Leung, a command to refresh can be delayed from a request to refresh. Page 2 paragraph [0013]. Because of this, refresh commands of different memory blocks can overlap, contrary to what is required by claim 6.

Because of the remarks herein regarding Claim 6 and the amendment and remarks to independent Claim 1, from which Claim 6 depends, the applicant asserts that the examiner's rejection of Claim 6 has been traversed and requests that Claim 6 be allowed.

Claim 8. The examiner has cited Leung as disclosing a memory system "wherein all memory blocks have a refresh controller contained therein which enable

sequential refresh of the subsequent memory blocks. (Page 2, Paragraphs [0014] and [0011])." Claim 8, as amended, states: "wherein all memory blocks have a refresh controller contained therein which enable sequential refresh of the subsequent memory blocks, such that no two memory blocks are refreshed at the same time." Leung neither discloses nor suggests that no two memory blocks are refreshed at the same time. While Leung discloses that refresh requests are daisy-chained (page 4, paragraph [0047]) and thus "sequential," as explained above, in the system disclosed by Leung, two memory blocks can be refreshed at the same time in which case the memory blocks are not refreshed sequentially.

By the claim amendment and the remarks herein, the applicant asserts that the examiner's rejection of independent Claim 8 has been traversed, and requests that Claim 8 be allowed as presently amended.

Claims 9, 10, 12 and 13. By the claim amendment to independent Claim 8 and the remarks regarding Claim 8 herein, the applicant asserts that the examiner's rejection of Claim 8 has been traversed, and requests that Claims 9, 10, 12 and 13, which depend from Claim 8, be allowed.

Claim 11. The examiner has cited Leung as disclosing "wherein the refresh controller of each memory block generates a refresh request [RFREQ] for an immediately subsequent memory block when the memory block it belongs to is being refreshed. (Page 4, paragraph [0047])." Leung does not disclose nor suggest that the

refresh controller of each memory block generates a refresh request for an immediately subsequent memory block when the memory block it belongs to is being refreshed. Leung discloses a daisy-chained series of "D" registers, (321, Fig. 3) one in each memory block, that sequentially clock refresh requests to each next memory block on every clock cycle. Page 4, paragraph [0047]. "The refresh request to the memory blocks is thus generated by a daisy chain formed by the D registers connecting to the REQI and REQO terminals of the memory blocks 1000-1127." Leung does not disclose that the sequential refresh request to the next sequential block occur while a first block is being refreshed. To the contrary, the refresh of any particular block can be delayed if there is a memory request to that block, yet the D register in the block will still cause the refresh out signal (REQO) to propagate to the next sequential block.

Because of the remarks herein regarding Claim 11 and the amendment and remarks to independent Claim 8, from which Claim 11 depends, the applicant asserts that the examiner's rejection of Claim 11 has been traversed and requests that Claim 11 be allowed.

Claim 14. The examiner has cited Leung as disclosing "wherein the refresh commands do not overlap in timing." (citing page 1 paragraph [0004] and page 2 paragraph [0013]). The overlap in timing prevented by Leung is between refresh cycles and external access to the memory, not between memory blocks. "Because an external access and a refresh access can be initiated at the same time, the DRAM array must be

able to handle both within the allowable access time so as to prevent the refresh access from interfering with the external access." Page 2, paragraph [0004]. Claim 14 requires that "the refresh commands for the memory blocks do not overlap in timing." While Leung discloses refresh requests that are daisy-chained (page 2 paragraph [13]) Leung does not disclose or suggest that the refresh commands for the memory blocks do not overlap in timing. In fact, in Leung, a command to refresh can be delayed from a request to refresh. Page 2 paragraph [0013]. Because of this, refresh commands of different memory blocks can overlap, contrary to what is required by claim 14.

Because of the remarks herein regarding Claim 14 and the amendment and remarks to independent Claim 8, from which Claim 14 depends, the applicant asserts that the examiner's rejection of Claim 14 has been traversed and requests that Claim 14 be allowed.

Claim 15. The examiner has cited Leung as disclosing "wherein the refresh controller provides a refresh address [101]." Claim 15 refers to a refresh controller, that is a part of each memory block. See independent claim 8, from which claim 15 depends. "wherein all memory blocks have a refresh controller contained therein. . . ." Leung [101] does not disclose or suggest a refresh controller contained in each memory block. To the contrary, Leung discloses "a central refresh address generator [that] increments the refresh address each time the refresh request signal is asserted." Page 2, paragraph 13. Because Leung does not disclose or suggest memory blocks that have a refresh

controller contained therein, wherein the refresh controller provides a refresh address, and because of the remarks applicable to independent claim 8, from which Claim 15 depends, the applicant asserts that the examiner's rejection of Claim 15 has been traversed and requests that Claim 15 be allowed.

Claim 16. The examiner has cited Leung as disclosing a dynamic random access memory system "wherein all memory blocks have a refresh controller contained therein which enable sequential refresh of the subsequent memory blocks. (Page 2, Paragraphs [0014] and [0011])." The applicant has amended Claim 16 to state the limitation: "wherein all memory blocks have a refresh controller contained therein which enable sequential refresh of the subsequent memory blocks, such that no two memory blocks are refreshed at the same time." Leung neither discloses nor suggests that no two memory blocks are refreshed at the same time. While Leung discloses that refresh requests are daisy-chained (page 4, paragraph [0047]) and thus "sequential," as explained above, in the system disclosed by Leung, two memory blocks can be refreshed at the same time in which case the memory blocks are not refreshed sequentially.

By the claim amendment and the remarks herein, the applicant asserts that the examiner's rejection of independent Claim 16 has been traversed, and requests that Claim 16 be allowed as presently amended.

Claims 17 and 19. By the claim amendment to independent Claim 16 and the

remarks regarding Claim 16 herein, the applicant asserts that the examiner's rejection of Claim 16 has been traversed, and requests that Claims 17 and 19, which depend from Claim 16, be allowed.

Claim 18. The examiner has cited Leung as disclosing "wherein the refresh controller of each memory block generates a refresh command for refreshing the memory block it belongs to and a refresh request [RFREQ] for an immediately subsequent memory block when the memory block it belongs to is being refreshed. (Page 4, paragraph [0047])." Leung does not disclose nor suggest that the refresh controller of each memory block generates a refresh request for an immediately subsequent memory block when the memory block it belongs to is being refreshed. Leung discloses a daisy-chained series of "D" registers, (321, Fig. 3) one in each memory block, that sequentially clock refresh requests to each subsequent memory block on every clock cycle. Page 4, paragraph [0047]. "The refresh request to the memory blocks is thus generated by a daisy chain formed by the D registers connecting to the REQI and REQO terminals of the memory blocks 1000-1127." Leung does not disclose that the sequential refresh request to the next sequential block occur while a first block is being refreshed. To the contrary, the refresh of any particular block can be delayed if there is a memory request to that block, yet the D register in the block will still cause the refresh out signal (REQO) to propagate to the next sequential block.

Because of the remarks herein regarding Claim 18 and the amendment and

remarks to independent Claim 16, from which Claim 18 depends, the applicant asserts that the examiner's rejection of Claim 18 has been traversed and requests that Claim 18 be allowed.

Claim 20. The examiner has cited Leung as disclosing "wherein the refresh commands do not overlap in timing." (citing page 1 paragraph [0004] and page 2 paragraph [0013]). The overlap in timing prevented by Leung is between refresh cycles and external access to the memory, not between memory blocks. "Because an external access and a refresh access can be initiated at the same time, the DRAM array must be able to handle both within the allowable access time so as to prevent the refresh access from interfering with the external access." Page 2, paragraph [0004]. Claim 20 requires that "the refresh commands for the memory blocks do not overlap in timing." While Leung discloses refresh requests that are daisy-chained (page 2 paragraph [13]) Leung does not disclose or suggest that the refresh commands for the memory blocks do not overlap in timing. In fact, in Leung, a command to refresh can be delayed from a request to refresh. Page 2, paragraph [0013]. Because of this, refresh commands of different memory blocks can overlap, contrary to what is required by claim 20.

Because of the remarks herein regarding Claim 20 and the amendment and remarks to independent Claim 16 from which Claim 20 depends, the applicant asserts that the examiner's rejection of Claim 20 has been traversed and requests that Claim 20 be allowed.

Claim 21. The examiner has cited Leung as disclosing "wherein the refresh controller provides a refresh address [101]." Claim 21 refers to a refresh controller, that is a part of each memory block. See independent claim 16, from which claim 21 depends. "wherein all memory blocks have a refresh controller contained therein. . . ." Leung [101] does not disclose or suggest a refresh controller contained in each memory block. To the contrary, Leung discloses "a central refresh address generator [that] increments the refresh address each time the refresh request signal is asserted." Page 2, paragraph [0013]. Because Leung does not disclose or suggest memory blocks that have a refresh controller contained therein, wherein the refresh controller provides a refresh address, and because of the remarks applicable to independent claim 16, from which Claim 21 depends, the applicant asserts that the examiner's rejection of Claim 21 has been traversed and requests that Claim 21 be allowed.

IV. Conclusion

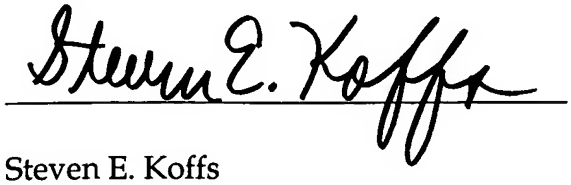
Having addressed the examiner's rejections, applicant submits that the reasons for the examiner's rejections have been overcome by the new claims and remarks made herein, and the rejections can no longer be sustained. Applicant respectfully requests reconsideration and withdrawal of the rejections and that a Notice of Allowance be issued.

Should any unresolved issues remain, the examiner is requested to call Applicant's attorney at the telephone number below.

The Commissioner for Patents is hereby authorized to charge any fees or credit

any excess payment that may be associated with this communication to Duane Morris LLP deposit account 04-1679.

Respectfully submitted,



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Amendments to the Drawings

Please replace Figures 1 – 3 with Replacement Sheets containing revised Figures 1 - 3 attached hereto. Each of the revised Figures is now labeled "PRIOR ART."